U.S. Patent Application No. 09/696,117

Inventor: Satoshi Kitagawa Filed: October 25, 2000

## REMARKS

In the above-identified Office Action, the Examiner has rejected claims 3-6, 13-23 and 26 under 35 U.S.C. § 103(a) as unpatentable over Huang in view of Yano and Oishi. The Examiner has stated that Huang teaches a method for identifying a wafer during its manufacture but fails to teach that a first mark is formed at a location spaced apart from the second mark. The Examiner has then stated that Yano teaches a method to be able to identify a wafer through manufacturing processes and it would have been obvious to employ a second mark having identical content at a spaced apart location but, this combination still fails to teach that the marks are formed on an interior wall of a notch in the semiconductor wafers. The Examiner finds this teaching in Oishi which teaches a wafer having a laser mark on a chamfered edge. The Examiner believes it would have been obvious to affix a mark on the interior wall surface of the notch because the notch is a somewhat protected area and hence the mark would be protected as well.

Applicant disagrees with the conclusions reached by the Examiner. Oishi teaches away from placing a mark on an interior wall surface of a notch, stating that the notched edge should be polished to specular glossiness in order to maintain Oishi's invention and that such polishing is troublesome and residual stresses inevitably remain near the notched part and it is difficult to completely remove these residual stresses. Thus, Oishi teaches placing his mark in a place where residual work stress or thermal stress on a wafer can be avoided, i.e. on the chamfered edge.

Further, Applicant believes that the Examiner is reading Yano as teaching that each individual mark in the bar code will be taken as a separate mark. Accordingly, Applicant has amended claim 26 so that the claim now reads "forming a first mark capable of identifying the said wafer." The individual marks in the bar code of Yano are not capable of identifying the wafer and accordingly, Applicant believes that Yano no longer can be stated to teach the provision of identical marks.

Further, Applicant teaches away from the method of Oishi in that Oishi teaches placing his identification marks on the outer circumference of the wafer and not within the notch. It is noted that the outer circumference of the wafer receives a mechanical interference and thus

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cracks and breakage can easily occur when the wafer is being polished. Accordingly, the mark formed on the outer circumference of the wafer can easily disappear while on the other hand the inner circumference of the notch is not easily affected by the mechanical interface of polishing and will maintain its presence on the wafer. As a result, the provision of two or more marks enhances the assurance of their presence and subsequent reading.

Applicant hereby requests reconsideration and reexamination thereof.

With the above amendments and remarks, this application is considered ready for allowance and Applicant earnestly solicits an early notice of same. Should the Examiner be of the opinion that a telephone conference would expedite prosecution of the subject application, he is respectfully requested to call the undersigned at the below-listed number.

Respectfully submitted,

November 8, 2004

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